Applicant: Louis A. Lippincott
Serial No.: 10/600,048
Filed: June 19, 2003
Title: COMMUNICATION PORTS IN A DATA DRIVEN ARCHITECTURE

Examiner: Hau H. Nguyen
Group Art Unit: 2628
Docket No.: 884.899US1
Customer Number: 21186

APPEAL BRIEF UNDER 37 CFR § 41.37

Mail Stop Appeal Brief- Patents
Commissioner for Patents
P.O. Box 1450
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Sir:

The Appeal Brief is presented in response to the rejection of claims 1-23 and 37-38 of the above-identified application, as set forth in the Final Office Action mailed February 19, 2008.

The Commissioner of Patents and Trademarks is hereby authorized to charge Deposit Account No. 19-0743 in the amount of $540.00 which represents the requisite fee set forth in 37 C.F.R. 41.20(b)(2). Appellant respectfully requests consideration and reversal of the Examiner's rejections of pending claims.

APPEAL BRIEF UNDER 37 C.F.R. § 41.37

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1. REAL PARTY IN INTEREST

The real party in interest of the above-captioned patent application is the assignee, Intel Corporation.

2. RELATED APPEALS AND INTERFERENCES

An Appeal Brief was filed on March 20, 2009 in the following related Application: Serial No. 10/600,047 "Processor to Processor Communication in a Data Driven Architecture", Applicant – Louis A. Lippincott, filed on June 19, 2003

3. STATUS OF THE CLAIMS

The present application was filed on July 19, 2003 with 30 claims. In response to the Office Action mailed September 2, 2005, an Amendment was filed to amend claim 10. In response to the Office Action mailed on April 28, 2006, an Amendment was filed to amend claims 1-2 and 5-6. In response to the Office Action mailed on October 16, 2006, an Amendment was filed to amend claims 1, 7, 13, 18 and 25 and to cancel claim 9, 11, 16, 20 and 26. Claims 1-8, 10, 12-15, 17-19, 21-25 and 27-30 stand rejected, remain pending, and are subject of the present Appeal.

4. STATUS OF AMENDMENTS

No amendments have been made subsequent to the Office Action dated April 17, 2008.

5. SUMMARY OF CLAIMED SUBJECT MATTER

Some aspects of the present inventive subject matter include, but are not limited to, methods, systems and apparatus for processor to processor communication in a data driven architecture. In claim 1, an apparatus includes a first processor having two or more processor elements and two or more input/output (I/O) ports coupled together by a first port ring that is within the first processor. See Figures 1-2 – image processor 102, image signal processors 202 and port rings 250 and page 7, line 1 – page 11, line 8. The apparatus also includes a second processor having two or more processor elements and two or more I/O ports coupled together by a second port ring that is within the second processor. See Figures 1-2 – image processor 102, image signal processors 202 and port rings 250 and page 7, line 1 – page 11, line 8. The second processor is coupled to the first processor through at least one I/O port of a third port ring within a third processor. See Figures 1-2 – image processor 102, image signal processors 202 and port rings 250 and page 7, line 1 – page 11, line 8. The two or more I/O ports in the first processor, the second processor and the third processor are configured to establish a logical connection between the first processor and the second processor. See Figure 10 – routes 1002, 1004, 1006, 1008 and 1010 of the logical connections and page 21, line 26 – page 27, line 9. The logical connection is to originate at first processor and to traverse through the third processor and to complete at the second processor. See Figure 10 – routes 1002, 1004, 1006, 1008 and 1010 of the logical connections and page 21, line 26 – page 27, line 9. The logical connection is established based on other active logical connections that include at least one of the first processor, the second processor and third processor. See Figure 10 – routes 1002, 1004, 1006, 1008 and 1010 of the logical connections and page 21, line 26 – page 27, line 9 and page 15, line 29 – page 16, line 4.

In claim 7, an apparatus includes a number of image signal processors coupled together in a point-to-point configuration. See Figures 1-2 – image processor 102, image signal processors 202 and port rings 250 and page 7, line 1 – page 11, line 8. One image signal processor of the number of image signal processors includes at least one processor element and a port ring, wherein the port ring includes a number of ports. See Figures 1-

2 – image processor 102, image signal processors 202 and port rings 250 and page 7, line 1 – page 11, line 8. A port of the number of ports coupled to the other ports of the port ring and to a port of a port ring of a different image signal processor. See Figures 1-2 – image processor 102, image signal processors 202 and port rings 250 and page 7, line 1 – page 11, line 8. The number of ports within the port rings of the number of image signal processors are configured to establish logical connections between the number of image signal processors. See Figure 10 – routes 1002, 1004, 1006, 1008 and 1010 of the logical connections and page 21, line 26 – page 27, line 9. The logical connections are to originate at a source image signal processor of the number of image signal processors and to traverse a number of intermediate image signal processors of the number of image signal processors. See Figure 10 – routes 1002, 1004, 1006, 1008 and 1010 of the logical connections and page 21, line 26 – page 27, line 9. The logical connections are to complete at a destination image signal processor of the number of image signal processors. See Figure 10 – routes 1002, 1004, 1006, 1008 and 1010 of the logical connections and page 21, line 26 – page 27, line 9. The source image signal processor is to transmit an initialize signal, prior to transmission of data along the logical connection, through the number of intermediate image signal processors to the destination image signal processor in the order that data is transmitted in the logical connection. See page 16, lines 5-18.

In claim 13, a system includes a Complementary Metal Oxide Semiconductor (CMOS) sensor to capture image data. See Figure 1 – sensor 116 and page 5, lines 2-11. The system also includes an image processor comprising a number of expansion interfaces and a number of image signal processors, wherein at least one expansion interface of the number of expansion interfaces is configured to receive the image data to be captured by the CMOS sensor. See Figures 1-2 – image processor 102, image signal processors 202 and expansion interfaces 208 and page 7, line 1 – page 11, line 8. At least one of the image signal processors of the number of image signal processors includes a processor element and a port ring having a number of input/output ports to couple the at least one image signal processor to other image signal processors in the image processor in a point-to-point configuration. See Figures 1-2 – image processor 102, image signal

processors 202 and port rings 250 and page 7, line 1 – page 11, line 8. The system also includes a host processor to configure a number of logical connections among the number of image signal processors. See Figures 1and 10 – host processor 108, routes 1002, 1004, 1006, 1008 and 1010 of the logical connections and page 21, line 26 – page 27, line 9. At least one logical connection is to originate at a source image signal processor of the number of image signal processors and to finish at a destination image signal processor of the number of image signal processors. See Figure 10 – routes 1002, 1004, 1006, 1008 and 1010 of the logical connections and page 21, line 26 – page 27, line 9. At least one logical connection includes traversal through a number of ports of the port rings of at least one intermediate image signal processor of the number of image signal processors between the source image signal processor and the destination image signal processor. See Figure 10 – routes 1002, 1004, 1006, 1008 and 1010 of the logical connections and page 21, line 26 – page 27, line 9.

In claim 18, a method includes registering a logical connection with a number of ports of port rings of a number of image signal processors in a logical connection based on transmission of an initialization signal through the logical connection. See Figure 11 – blocks 1102, 1104 and 1106 and page 27, line 15 – page 28, line 22. The method also includes executing an image process operation. See Figure 12 – block 1204 and page 29, lines 13-30. The method includes forwarding an output of the image process operation through ~~a~~ the logical connection that includes a data path through ~~a~~ the number of ports of port rings of the number of image signal processors, independent of image process operations in the number of image signal processors. See Figure 12 – block 1206 and page 30, lines 1-8.

In claim 22, a method includes receiving configuration data for a logical connection established for transmission of image data from a source image signal processor to a destination image signal processor through a number of intermediate image signal processors. See Figure 11, block 1102 and page 27, lines 15-25. The method also includes registering the logical connection with ports of the source image signal processor, the destination image signal processor and the number of intermediate image signal processors. See Figure 11, block 1104 and page 27, line 26 – page 28, line 8. The

method also includes routing the image data through the ports of the logical connection, subsequent to registering the logical connection and independent of image process operations by processing elements within the number of intermediate image signal processors. See Figure 12 – block 1206 and page 30, lines 1-8.

This summary does not provide an exhaustive or exclusive view of the present subject matter, and Appellant refers to the appended claims and its legal equivalents for a complete statement of the invention.

6. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 25 and 27-30 were rejected under 35 USC § 101 because the claimed invention is directed to non-statutory subject matter. Claims 1-8, 10, 12, 18, 19, 21-25 and 27-30 were rejected under 35 USC § 103(a) as being unpatentable over Tulpule et al. (U.S. 4,933,836) (hereinafter Tulpule) in view of Galicki et al. (U.S. 6,967,950) (hereinafter Galicki). Claims 13-15 and 17 were rejected under 35 USC § 103(a) as being unpatentable over Tulpule in view of Galicki and further in view of Hsieh et al. (U.S. 6,757,019).

7. ARGUMENT

A) Discussion of the rejection of claims 25 and 27-30 were rejected under 35 U.S.C. § 101 because the claimed invention is directed to non-statutory subject matter.

Applicant has canceled claims 25 and 27-30 in accordance with 37 CFR 41.37. Applicant respectfully submits that such claims are independent of the remaining claims and thus does not affect the scope of any other pending claim in the proceeding. Therefore, the rejection of claims 25 and 27-30 is moot.

B) The Applicable Law for Rejection under 35 U.S.C. § 103

The Examiner has the burden under 35 U.S.C. § 103 to establish a *prima facie* case of obviousness. *In re Fine*, 837 F.2d 1071, 1074, 5 U.S.P.Q.2d (BNA) 1596, 1598 (Fed. Cir. 1988). As discussed in KSR International Co. v. Teleflex Inc. et al. (U.S. 2007), the determination of obviousness under 35 U.S.C. § 103 is a legal conclusion based on factual evidence. *See Princeton Biochemicals, Inc. v. Beckman Coulter, Inc.*, 7, 1336-37 (Fed. Cir. 2005). The legal conclusion, that a claim is obvious within § 103(a), depends on at least four underlying factual issues set forth in *Graham v. John Deere Co. of Kansas City*, 383 U.S. 1, 17 (1966): (1) the scope and content of the prior art; (2) differences between the prior art and the claims at issue; (3) the level of ordinary skill in the pertinent art; and (4) evaluation of any relevant secondary considerations.

The *KSR* Court further held that "rejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." (*See In re Kahn*, 441 F. 3d 977, 988 (CA Fed. 2006) cited with approval in *KSR Int'l v. Teleflex Inc.*, 127 S. Ct. 1727, 1740-41 (2007)).

Therefore, the test for obviousness under §103 must take into consideration the invention as a whole; that is, one must consider the particular problem solved by the combination of elements that define the invention. (*Interconnect Planning Corp. v. Feil,*

774 F.2d 1132, 1143, 227 USPQ 543, 551 (Fed. Cir.1985).) The Examiner must, as one of the inquiries pertinent to any obviousness inquiry under 35 U.S.C. §103, recognize and consider not only the similarities but also the critical differences between the claimed invention and the prior art. (*In re Bond, 910* F.2d 831,834, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990), *reh'g denied,* 1990 U.S. App. LEXIS 19971 (Fed. Cir.1990).) Critical differences in the prior art must be recognized (when attempting to combine references). (*In re Bond,* 910 F.2d 831,834, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990), *reh'g denied,* 1990 U.S. App. LEXIS 19971 (Fed. Cir.1990).)

Moreover, the fact that a reference teaches away from a claimed invention is highly probative that the reference would not have rendered the claimed invention obvious to one of ordinary skill in the art. (*Stranco Inc. v. Atlantes Chemical Systems, Inc.,* 15 USPQ2d 1704, 1713 (Tex. 1990).) When the prior art teaches away from combining certain known elements, discovery of a successful means of combining them is more likely to be nonobvious. (*Id.* at 4 citing *United States v. Adams,* 383 U.S. 39, 51-51 (1966).)

"If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims prima facie obvious." (*In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959). The CCPA has also noted that "[t]he court must be ever alert not to read obviousness into an invention on the basis of the applicant's own statements; that is, we must view the prior art without reading into that art appellant's teachings." *In re Sponnoble,* 160 USPQ 237, 243 (CCPA 1969). These principles have not been changed by the ruling in *KSR*.

C) Discussion of the rejection of claims 1-8, 10, 12, 18, 19, 21-25 and 27-30 under 35 U.S.C. § 103(a) as being unpatentable over Tulpule in view of Galicki and claims 13-15 and 17 under 35 U.S.C. § 103(a) as being unpatentable over Tulpule in view of Galicki and further in view of Hsieh.

Applicant respectfully traverses the rejections.

Claims 1-6

Claim 1 recites "wherein the logical connection is established based on other active logical connections that include at least one of the first processor, the second processor and third processor." The Office indicated that Galicki discloses this limitation. In particular, the Office indicated that the active receive channels in FIGS. 7-9 and col. 8, lines 48-56 of Galicki discloses this limitation. Further, the Office indicated that Galicki teaches more than one logical connection between processors citing col. 5, lines 48-62. Also, the Office indicated that the depending on other logical connections is disclosed in FIG. 6, col. 6, lines 43-55. These sections of Galicki do relate to a packet transfer between two processors. However, neither Tulpule or Galicki, alone or in combination, disclose or suggests that a logical connection is established base on other active logical connections among processors. Specifically, in Galicki, a data packet is received into a bridge and the packet is routed based on the data in the header ("[d]epending on the header evaluation, the point-to-point and cell packets may be routed out the bridge through left port 601, right port 602 or center port 603." Galicki at col. 6, lines 49-53). However, neither reference discloses or suggest establishing based on other active logical connection among the processors.

Accordingly, the cited art does not disclose or suggest all of the claim limitations of claim 1. Applicant respectfully submits that the rejection of claim 1 under 35 U.S.C. §103 has been overcome. Claims 2-6 depend from claim 1 and distinguishes the reference for at least the same reason.

Claims 7, 8, 10 and 12

Claim 7 recites "wherein the source image signal processor is to transmit an initialize signal, prior to transmission of data along the logical connection, through the number of intermediate image signal processors to the destination image signal processor in the order that data is transmitted in the logical connection." The Office indicated that this limitation was disclosed by Galicki by the packet header, citing col. 5, lines 49-61 and col. 8, lines 48-56. Applicant respectfully traverses. These recited sections of

Galicki do relate to packet routing using the packet header. Applicant respectfully submits that a data packet that is routed based on information in its header does not disclose or suggest the transmission of an initialization signal prior to transmission of the data along the logical connection.

In particular, Galicki at col. 5, lines 49-61 and col. 8, lines 48-56 is relating to actual data transmission based on routing information in the header of the packet. Galicki describes the packet to include a header, the data and a tail:

> A transfer packet is formed when a packet header is injected into the datapipe network, followed by the data block itself and then a tail.

Galicki at col. 7, lines 30-32.

These sections of Galicki do not disclose or suggest an initialization signal along a logical connection prior to the actual data transmission.

Accordingly, the cited art does not disclose or suggest all of the claim limitations of claim 7. Applicant respectfully submits that the rejection of claim 7 under 35 U.S.C. §103 has been overcome. Claims 8, 10 and 12 depend from claim 7 and distinguishes the reference for at least the same reason.

Claims 13-15, 17-19, 21-25 and 27-30

With regard to claims 13-15, 17-19, 21-25 and 27-30, Applicant respectfully submits that the Office Action did not make out a *prima facie* case of obviousness because even if combined, the cited references fail to teach or suggest all of the elements of claims 13-15, 17-19, 21-25 and 27-30. In particular, for at least the reasons set forth above regarding claims 1 and 7, Applicant respectfully submits that the cited references fail to teach or suggest all of the elements of claims 13-15, 17-19, 21-25 and 27-30. Accordingly, Applicants respectfully submit that the rejection of claim 13-15, 17-19, 21-25 and 27-30 under 35 U.S.C. §103 has been overcome.

8. SUMMARY

It is respectfully submitted that the claims are patentable over the cited art. Reversal of the rejection and allowance of the pending claim are respectfully requested.

Respectfully submitted,

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Date April 17, 2009

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: MS Appeal Brief – Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 17th day of April, 2009.

Amy Moriarty
Name

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Signature

CLAIMS APPENDIX

1. An apparatus comprising:

a first processor having two or more processor elements and two or more input/output (I/O) ports coupled together by a first port ring that is within the first processor; and

a second processor having two or more processor elements and two or more I/O ports coupled together by a second port ring that is within the second processor, wherein the second processor is coupled to the first processor through at least one I/O port of a third port ring within a third processor, wherein the two or more I/O ports in the first processor, the second processor and the third processor are configured to establish a logical connection between the first processor and the second processor, the logical connection to originate at first processor and to traverse through the third processor and to complete at the second processor, wherein the logical connection is established based on other active logical connections that include at least one of the first processor, the second processor and third processor.

2. The apparatus of claim 1, wherein the two or more I/O ports of the first processor is not directly connected to the two or more I/O ports of the second processor.

3. The apparatus of claim 1, wherein the first processor, the second processor and the third processor are part of a number of processors in a point-to-point configuration.

4. The apparatus of claim 1, wherein the first processor is configured to transmit output from an image process operation to the second processor through the at least one I/O port of the port ring of the third processor based on a logical connection.

5. The apparatus of claim 4, wherein the two or more I/O ports of the first processor, the two or more I/O ports of the second processor and the at least one I/O port of the third processor comprise a First-In-First-Out memory.

6. The apparatus of claim 5, wherein the two or more I/O ports of the first processor, the two or more I/O ports of the second processor and the at least one port of the third processor comprise a receiver port and a transmitter port, wherein the first processor is configured to transmit the output based on a handshake protocol among the receiver ports and the transmitter ports of the first processor, the second processor and the third processor.

7. An apparatus comprising:

a number of image signal processors coupled together in a point-to-point configuration, wherein one image signal processor of the number of image signal processors includes at least one processor element and a port ring, wherein the port ring includes a number of ports, a port of the number of ports coupled to the other ports of the port ring and to a port of a port ring of a different image signal processor, wherein the number of ports within the port rings of the number of image signal processors are configured to establish logical connections between the number of image signal processors, wherein the logical connections are to originate at a source image signal processor of the number of image signal processors and to traverse a number of intermediate image signal processors of the number of image signal processors and to complete at a destination image signal processor of the number of image signal processors, wherein the source image signal processor is to transmit an initialize signal, prior to transmission of data along the logical connection, through the number of intermediate image signal processors to the destination image signal processor in the order that data is transmitted in the logical connection.

8. The apparatus of claim 7, wherein the at least one processor element in a first of the number of image signal processors is configured to perform one of a number of image process-based operations.

10. The apparatus of claim 9, wherein the at least one processor element is configured to output a result of the one of the number of image process-based operations to a different processor element in a different image signal processor through one of the logical connections.

12. The apparatus of claim 9, wherein the number of ports include a storage memory for storage of data between communicated among the number of image processors through the configured logical connections.

13. A system comprising:

a Complementary Metal Oxide Semiconductor (CMOS) sensor to capture image data;

an image processor comprising a number of expansion interfaces and a number of image signal processors, wherein at least one expansion interface of the number of expansion interfaces is configured to receive the image data to be captured by the CMOS sensor, wherein at least one image signal processor of the number of image signal processors comprises a processor element and a port ring having a number of input/output ports to couple the at least one image signal processor to other image signal processors in the image processor in a point-to-point configuration; and

a host processor to configure a number of logical connections among the number of image signal processors, wherein at least one logical connection is to originate at a source image signal processor of the number of image signal processors and to finish at a destination image signal processor of the number of image signal processors, wherein the at least one logical connection includes traversal through a number of ports of the port rings of at least one intermediate image signal processor of the number of image signal

processors between the source image signal processor and the destination image signal processor.

14. The system of claim 13, wherein the at least one image signal processor comprises a hardware accelerator to execute image process operations.

15. The system of claim 13, wherein the image processor comprises a global bus coupled to the number of expansion interfaces and the number of image signal processors, independent of the point-to-point configuration among the number of image signal processors.

17. The system of claim 13, wherein traversal through the number of ports of the port rings of the at least one intermediate image signal processor is independent of image process operations by processor elements within the at least one intermediate image signal processor.

18. A method comprising:

registering a logical connection with a number of ports of port rings of a number of image signal processors in a logical connection based on transmission of an initialization signal through the logical connection;

executing an image process operation; and

forwarding an output of the image process operation through ~~a~~ the logical connection that includes a data path through ~~a~~ the number of ports of port rings of ~~a~~ the number of image signal processors, independent of image process operations in the number of image signal processors.

19. The method of claim 18, wherein forwarding the output of the image process operation through the logical connection from one of the number of image signal processors to a different one of the number of image signal processors comprises,

transmitting a request signal from a transmitter port of the one of the number of image signal processors to a receiver port of the different one of the number of image signal processors; and

receiving, in response to the request signal, a grant signal from the receiver port to the transmitter port.

21. The method of claim 18, wherein forwarding the output of the image process operation through the logical connection that includes the data path through the number of ports of the port rings of the number of image signal processors comprises forwarding the output of the image process operation through the logical connection that includes the data path through the number of ports of the port rings of the number of image signal processors, wherein the number of image signal processors are connected together through the number of ports in a point-to-point configuration.

22. A method comprising:

receiving configuration data for a logical connection established for transmission of image data from a source image signal processor to a destination image signal processor through a number of intermediate image signal processors;

registering the logical connection with ports of the source image signal processor, the destination image signal processor and the number of intermediate image signal processors; and

routing the image data through the ports of the logical connection, subsequent to registering the logical connection and independent of image process operations by processing elements within the number of intermediate image signal processors.

23. The method of claim 22, wherein registering the logical connection with the ports of the source image signal processor, the destination image signal processor and the number of intermediate image signal processors comprises transmitting an initialize signal that is transmitted along a path of the logical connection that the image data is routed.

24. The method of claim 22, wherein registering the logical connection with the ports of the source image signal processor, the destination image signal processor and the number of intermediate image signal processors comprises registering point-to-point connections between the ports of the logical connection.

25. (Canceled)

27-30. (Canceled)

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.